DAE

**IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE**

Appl. No.: 10/005,513

Applicant(s): James J. Brogle et al.

Filed: November 8, 2001

Title: MONOLITHICALLY INTEGRATED PIN DIODE AND SCHOTTKY DIODE CIRCUIT AND METHOD OF FABRICATING SAME

TC/A.U.: 2800/2823

Examiner: George G. Fourson, III

Atty. Docket: Tyco.002

CERTIFICATE OF MAILING OR TRANSMISSION

I certify that this correspondence is being:

[X] deposited with the U.S. Postal Service with sufficient postage as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450; and

[X] transmitted by facsimile to Technology Center 2800 at the U.S. Patent and Trademark Office at 703-746-3942.

On: 9 December 2003

By: Michelle Welgoss
Michelle Welgoss

SUBMISSION UNDER 37 C.F.R. §1.8(b) TO REVIVE HOLDING OF ABANDONMENT AND REQUEST FOR ENTRY OF AMENDMENT UNDER 37 C.F.R. §1.111 AND INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Abandonment was mailed on November 18, 2003 in the above-captioned application. The Notice of Abandonment indicates that Applicants failed to respond in a timely manner to the Office Action mailed on April 1, 2003. For the reasons set forth below, Applicants respectfully request that the holding of abandonment be withdrawn, and the enclosed copy of the Amendment and IDS filed on July 1, 2003 be entered as timely.

An Information Disclosure Statement (IDS) and an Amendment under 37 C.F.R. §1.111 were sent by facsimile transmission to Technology Center 2800 of the U.S. Patent and Trademark Office at facsimile number (703) 872-9318. The Amendment and the IDS each included a Certificate of Mailing or Facsimile

Transmission compliant with 37 C.F.R. §1.8 and each were executed on July 1, 2003 by the undersigned attorney's assistant, Michelle Welgoss. The items sent by facsimile were: a two (2) page Transmittal of Information Disclosure Statement; a one (1) page Information Disclosure Citation; an eight (8) page reference (U.S. Patent 6,329,702 B1); and a thirteen (13) page Amendment Under 37 C.F.R. §1.111, for a total of twenty-four (24) pages. Upon completion of the transmission, a Transmission Verification Report was received indicating that 24 pages were transmitted to facsimile number (703) 872-9318. Moreover, an Auto-Reply Facsimile Transmission was received from the U.S. Patent and Trademark Office indicating that a total of twenty-four (24) pages were transmitted on July 1, 2003. Copies of the IDS, Amendment, the Transmission Verification Report and the Auto-Reply Facsimile Transmission are included. Finally, it is noted that a review of the records of Deposit Account 50-0238 does not show that the fee for the IDS under 37 C.F.R. §1.17 was charged.

It is respectfully submitted that the IDS and Amendment Under 37 C.F.R. §1.111 were filed in compliance with 37 C.F.R. §1.6(d) and 37 C.F.R. §1.8 on July 1, 2003. Therefore, it is respectfully submitted that a proper response under 37 C.F.R. §1.111 was timely filed in response to the Office Action of April 1, 2003. As such, it is respectfully requested that the holding of abandonment be withdrawn and it is respectfully requested that the Amendment Under 37 C.F.R. §1.111 and IDS filed on July 1, 2003 be entered and considered by the Office.

The undersigned attorney notes that the present Submission and accompanying materials is being sent by facsimile transmission directly to Supervisory Primary Examiner Olik Chaudhuri to facsimile number (703)746-3942 at Mr. Chaudhuri's request. Moreover, this request and copies of the accompanying

materials are being sent by First Class Mail Under 37 C.F.R. §1.8 on even date.

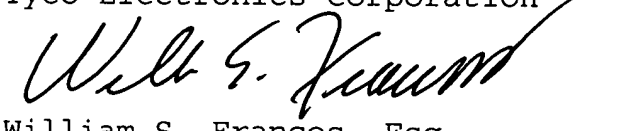
CONCLUSION

For at least the reasons set forth above, it is respectfully submitted that a timely response was filed in response to the Office Action of April 1, 2003. Therefore, it is respectfully submitted that the Holding of Abandonment was in error, and should be withdrawn. Entry and further and favorable consideration of the present application is respectfully submitted.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees including, but not limited to, the fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted on behalf of:
Tyco Electronics Corporation



William S. Francos, Esq.
Reg. No. 38,456

Date: December 9, 2003

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Enclosures

**IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE**

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On: 1 July 2003
By: Michelle Welgoss
Michelle Welgoss

Amendment Under 37 C.F.R. 1.111

Honorable Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated April 1, 2003, please amend the above referenced application as follows and reconsider the application in light of the following remarks.

This paper includes (each beginning on a separate sheet):

1. **Amendments to the Claims** are reflected in the listing of claims, which begins on page 3 of this paper.
2. **Remarks/Discussion of Issues** begin on page 7 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-16. (Cancelled).

17. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device, comprising:

a silicon substrate;

a plurality of first mesa portions disposed over the substrate;

a plurality of second mesa portions disposed over the substrate;

a plurality of PIN diodes each including a PIN anode region, wherein each one of the plurality of PIN diodes is disposed over a respective one of the plurality of first mesa portions;

a plurality of Schottky diodes each including a Schottky anode region, wherein one of the plurality of Schottky diodes is disposed over a respective one of the plurality of second mesa portions; and

a passivation layer disposed over the substrate, the passivation layer substantially covering the plurality of PIN diodes, the plurality of Schottky diodes, the plurality of first mesa portions, and the plurality of second mesa portions, while providing access to at least the PIN anode regions and the Schottky anode regions,

wherein the PIN anode regions are substantially co-planar with the Schottky anode regions.

18. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device of claim 17 wherein the passivation layer comprises a low-loss glass passivation layer.

19. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device of claim 17 wherein each of the Schottky anode regions include an epitaxial layer.

20. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device of claim 19 wherein the epitaxial layer of each of the Schottky anode regions has a thickness of approximately 0.1 μm.

21. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device, comprising:

a silicon substrate;

a first mesa portion and a second mesa portion, the first and second mesa portions being disposed over the substrate;

a PIN diode including a PIN anode region, the PIN diode being disposed over the first mesa portion;

a Schottky diode including a Schottky anode region, the Schottky diode being disposed over the second mesa portion; and

a passivation layer disposed over the substrate, the passivation layer substantially covering the PIN diode, the Schottky diode, the first mesa portion, and the second mesa

portion, while providing access to at least the PIN anode region and the Schottky anode region,

wherein the PIN anode region is substantially co-planar with the Schottky anode region.

22. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device of claim 21 wherein the passivation layer comprises a low-loss glass passivation layer.

23. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device of claim 21 wherein the Schottky anode region includes an epitaxial layer.

24. (Newly Added) A microwave/millimeter-wave monolithic integrated circuit device of claim 23 wherein the epitaxial layer of the Schottky anode region has a thickness of approximately 0.1 μm.

25. (Newly Added) A method of fabricating a microwave/millimeter-wave monolithic integrated circuit device including at least one PIN diode and at least one Schottky diode, the method comprising:

providing a silicon substrate;

forming at least one first mesa portion and at least one second mesa portion on the substrate;

forming the at least one PIN diode including a PIN anode in a PIN diode region of the substrate, the at least one PIN diode being formed on the at least one first mesa portion;

forming the at least one Schottky diode including a

Schottky anode in a Schottky diode region of the substrate, the at least one Schottky diode being formed on the at least one second mesa portion, the Schottky anode being formed in approximately the same plane as the PIN anode; and

depositing a passivation layer on the substrate to substantially cover the at least one PIN diode, the at least one Schottky diode, the at least one first mesa portion, and the at least one second mesa portion while providing access to at least the PIN anode and the Schottky anode.

26. (Newly Added) A method of claim 25 wherein the depositing step includes depositing a low-loss glass passivation layer on the substrate.

27. (Newly Added) A method of claim 25 wherein the forming the at least one first mesa portion and the at least one second mesa portion further includes performing a single anisotropic etching operation.

28. (Newly Added) A method of claim 27 wherein the forming the at least one first mesa portion and the at least one second mesa portion further comprises: depositing a layer of silicon nitride on the PIN diode region and the Schottky diode region of the substrate; masking portions of the PIN diode region and the Schottky diode region that are to become the at least one first mesa portion and the at least one second mesa portion; etching the silicon nitride layer except in the masked portions of the PIN diode region and the Schottky diode region, and conducting the single anisotropic etching

operation to form the at least one first mesa portion and the at least one second mesa portion on the substrate.

29. (Newly Added) A method of claim 25 wherein forming the PIN diode including a PIN anode furthercomprises: etching an implant window for the PIN anode in the PIN diode region of the substrate while masking the Schottky diode region of the substrate; and implanting a dopant through the implant window for the PIN anode in the PIN diode region of the substrate while masking the Schottky diode region of the substrate.

30. (Newly Added) A method of claim 25 wherein the forming the at least one Schottky diode including the Schottky anode further includes forming the Schottky anode subsequent to the deposition of the passivation layer.

31. (Newly Added) A method of claim 30 wherein the forming the at least one Schottky diode including the Schottky anode further includes forming an epitaxial layer of the Schottky anode in the Schottky diode region of the substrate by an ultra-high vacuum chemical vapor deposition process while masking the PIN diode region of the substrate.

32. (Newly Added) A method of claim 31 the forming the at least one Schottky diode including the Schottky anode further comprises forming the epitaxial layer of the Schottky anode at a temperature less than a transition temperature of the passivation layer.

REMARKS/DISCUSSION OF ISSUES

Upon entry of the present amendment, claims 17-32 are pending in the present application. Claims 17, 21 and 25 are the independent claims. Claims 1-16 have been cancelled without prejudice or disclaimer of their subject matter.

Claim Objections

In the Office Action dated April 1, 2003, claims 4 and 7 were objected to under 37 C.F.R.§ 1.75(c). This objection is moot in view of the present amendment.

Rejection Under 35 USC § 112 ¶ 2

Claims 3,5,6 and 11-16 were rejected under 35 USC § 112 ¶ 2 as being indefinite for failing to particularly point out and distinctly claim the subject matter that which applicants regard as the invention. While these claims have been cancelled, some of their subject matter has been incorporated into newly added claims. As such, these rejections are addressed as necessary.

The specific limitations that served as the bases of the rejections of claims 5, 11, 12, 13, 14-16 as set forth in items 6-11 of page 3 of the Office Action are not included in the newly added claims. As such, these rejections are moot.

However, applicants respectfully traverse the rejection of claim 3 for its inclusion of the term 'low-loss' glass. This limitation is included in newly added claim 18. The Office Action asserts that the term 'low-loss' is a relative term, which is not defined by the claim. Moreover, the Office Action asserts that one of ordinary skill in the art would not be reasonably

apprised of the scope of the invention. Applicants respectfully disagree.

The present application relates to integrated circuits (IC's) that can function at millimeter-wave and microwave frequencies. At these relatively high frequencies, losses can have a deleterious impact on power and performance in general. As such, it is beneficial to include materials in the IC's that aid in mitigating losses. Certainly, one of ordinary skill in the art of high-speed IC's would recognize the meaning and scope of the term 'low-loss' as it relates to a material of the IC. In furtherance to this point, applicants reference U.S. Patent 6,329,702, which includes the disclosure of the use of 'low-loss glass' in a high frequency IC. The disclosure of the '702 patent offers the use of borosilicate glass as a low-loss glass. Clearly, one skilled in the art at the time the present invention was made would have understood the meaning of the term 'low-loss' as it relates to glass in IC's; and the types of materials used to meet this need.

Accordingly, for at least the reasons set forth above, the rejections under 35 U.S.C. § 112, second paragraph are moot.

Rejections Under 35 USC § 102(b)

The Office rejects claims 1-4,8-10 and 14 under 35 USC § 102(b) as being anticipated by the *Calligaro, et al.* (U.S. Patent No. 5,102,822). First, the cancellation of claims 1-4, 8-10 and 14 renders the rejections of these claims moot. As these rejections may apply to any of newly added claims 17-32, applicants' position presented below applies.

Newly added independent claims 17, 21 and 25, and the claims

that depend therefrom are patentable over *Calligaro, et al.* for at least the reasons that follow.

To properly establish a *prima facie* case of anticipation, *all* of the claimed elements must be found in the prior art. It follows, therefore, that if a *single* claimed element is not found in the prior art, a *prima facie* case of anticipation cannot properly be established.

Claims 17 and 21 are drawn to a microwave/millimeter-wave monolithic integrated circuit device, and includes in combination "*... a silicon substrate...*".

Claim 25 is drawn to a method of fabricating a microwave/millimeter-wave monolithic integrated circuit device, and includes in combination "*...providing a silicon substrate...*"

In contrast to that which is set forth in applicants' independent claims, the reference to *Calligaro, et al.* lacks as teaching or suggestion of a silicon substrate in a device, or the providing of a silicon substrate in a method of manufacture.

In fact, the reference to *Calligaro, et al.* specifically recites that materials to which the invention of *Calligaro, et al.* may apply are group III-V materials such as GaAs. The substrate used in the device of the reference is semi-insulating (SI) GaAs, which is within a different realm of semiconductor devices, and is wholly inapplicable to the silicon-based technology of the present application. (Please refer to column 1, lines 17-19; column 3, lines 31-32; and Fig. 2 for support for these assertions.)

Accordingly, the reference to *Calligaro, et al.* lacks the teaching of a silicon substrate, as is claimed, and as the Office Action asserts. Therefore, because the reference to *Calligaro,*

et al. specifically lacks at least one of the limitations of independent claims 17, 21 and 25, these claims and the claims that depend directly or indirectly therefrom are allowable over the applied art. Allowance is earnestly solicited.

Rejections Under 35 U.S.C. § 103(a)

The Office rejects claims 5,6, 11-13 and 15-16 under 35 U.S.C. § 103(a) as being unpatentable over *Calligaro, et al.* in view of applied secondary and tertiary references.

First, the cancellation of claim 5,6, 11-13 and 15-16 renders the rejections of these claims moot. As these rejections may apply to any of newly added claims 17-32, applicants' position presented below applies.

The establishment of a *prima facie* case of obviousness under 35 USC § 103(a) requires that *all* of the elements be found in the prior art. It follows that if a *single* claimed element is not found in the prior art, a *prima facie* case of obviousness cannot be established. Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is a teaching, suggestion or motivation to do so found in the references relied upon. However, hindsight in never an appropriate motivation for combining references and/or the requisite knowledge available to one having ordinary skill in the art. To this end, relying upon hindsight knowledge of applicants' disclosure when the prior art does not teach nor suggest such knowledge results in the use of the invention as a template for its own reconstruction. This is wholly improper in the determination of patentability.

For the reasons set forth above, and while in no way

conceding as to the propriety of the combinations of references, or that the features of the newly added claims are within the teachings of the applied art, applicants assert that because independent claims 17 and 21 are allowable over the applied art, the claim that depend directly or indirectly therefrom are also allowable. Allowance is earnestly solicited.

Conclusion

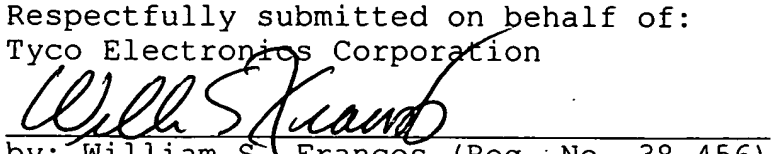
In view of the foregoing, Applicant respectfully requests withdrawal of the above noted rejection of record, the allowance of all pending claims, and the holding of this application in condition for allowance.

If any points remain of issue that may best be resolved through a personal or telephonic interview, the Office is respectfully requested to contact the undersigned at the telephone number listed below.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted on behalf of:
Tyco Electronics Corporation



by: William S. Francos (Reg. No. 38,456)

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Two Meridian Blvd.
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(610) 375-3513

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. Tyco.002

In Re Application Of: James J. Brogle et al.

Serial No.	Filing Date	Examiner	Group Art Unit
10/005,513	11/8/2001	Unknown	2823

Title: MONOLITHICALLY INTEGRATED PIN DIODE AND SCHOTTKY DIODE CIRCUIT AND METHOD OF FABRICATING SAME

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☐ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☒ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☒ the fee set forth in 37 CFR 1.17(p).

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. Tyco.002

In Re Application: **James J. Brogle et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
10/005,513	11/8/2001	Unknown	2823

MONOLITHICALLY INTEGRATED PIN DIODE AND SCHOTTKY DIODE CIRCUIT AND METHOD OF FABRICATING SAME

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

☐ A check in the amount of is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. **50-0238** as described below.

- ☒ Charge the amount of **$180.00**
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July 1, 2003
(Date)

Michelle Welgoss

Signature

Michelle Welgoss

Typed or Printed Name of Person Signing Certificate

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Typed or Printed Name of Person Mailing Certificate

***This certificate may only be used if paying by deposit account.**

Willis S. Francis

Signature

Dated: **July 1, 2003**

cc:

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Opti	Application Number
Tyc.. 02	10/005,513
Applicant(s)	
James J. Brogle et al.	
Filing Date	**Group Art Unit**
11/8/2001	2838

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,329,702	12/11/2001	Gresham et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

TRANSMISSION VERIFICATION REPORT

TIME : 07/01/2003 13:34
NAME : VOLENTINE FRANCOS
FAX : 6103758380
TEL : 6103753513

DATE,TIME	07/01 13:28
FAX NO./NAME	17038729318
DURATION	00:06:48
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RESULT	OK
MODE	STANDARD ECM

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.
Tyco.002

In Re Application Of: **James J. Brogle et al.**

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☐ the statement specified in 37 CFR 1.97(e);

OR